A 1-GSPS CMOS Flash A/D Converter for System-on-Chip Applications*

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Abstract

This paper presents an ultrafast CMOS flash A/D converter design and performance. Although the featured A/D converter is designed in CMOS, the performance is compatible to that of GaAs technology currently available. To achieve high-speed in CMOS, the featured A/D converter utilizes the Threshold Inverter Quantization (TIQ) technique. A 6-bit TIQ based flash A/D converter was designed with the 0.25 μm standard CMOS technology parameter. It operates with sampling rates up to 1 GSPS, dissipates 66.87mW of power at 2.5 V, and occupies 0.013 mm^2 area. The proposed A/D converter is suitable for System-on-Chip (SOC) applications in wireless products and other ultra high speed applications.

1. Introduction

One of the major challenges in developing a complete System-on-Chip (SOC) product for the wireless digital network market is the integration of radio frequency (RF) analog circuit components, mostly passive discrete components. The RF front-end components can be substantially reduced with a high-speed A/D converter and a high-speed digital processor, making possible the single-chip all-CMOS radio. Ultrafast A/D Converters are in demand, especially with portable wireless devices that use the radio frequency (RF) signal for networking.

Among known high-speed A/D converter architectures, the two most common implementations are the flash type and the pipeline type architectures. The flash type A/D converter is the faster of the two, but limited to lower resolution due to a large number of components (requiring $2^n - 1$ comparators for an n-bit A/D converter). The pipeline A/D converter is the slower of the two architectures, but is more suitable for higher resolution [9], requiring only n stages for an n-bit A/D converter.

The speed of an A/D converter is also affected by the type of solid-state technology used to implement the converter. Three different types of solid-state technologies are available for high-speed A/D converter implementation: the CMOS technology, the bipolar technology, and the Gallium Arsenide (GaAs) technology. The GaAs technology[1, 4, 5, 7] is the fastest of the three and the CMOS technology is the slowest. The ultrafast A/D converters are implemented with flash type architecture using the GaAs technology.

The current GaAs technology is not compatible with the silicon based CMOS technology, which makes it very difficult to realize the single-chip system solution aimed by the current SOC trend. For this reason, the authors propose an ultrafast CMOS flash A/D converter design [2, 6, 8, 10] featuring the Threshold Inverter Quantization (TIQ) technique. The TIQ technique allows faster A/D conversion speed using the standard CMOS logic circuitry preferred for SOC implementation.

The bipolar transistor technology allows faster operation and it is compatible with the CMOS technology. However, the BiCMOS technology requires more processing steps and higher cost compared to standard CMOS technology. Mixed-signal circuit implementation using only the standard CMOS technology is the preferred choice for the SOC products.

The main advantage of the proposed A/D converter design based on the TIQ technique is a simpler comparator design. The idea is to use the digital inverter as an analog voltage comparator. This eliminates the need for high-gain differential input voltage comparators that are inherently more complex and slower than the digital inverters. It also eliminates the need of reference voltages requiring a resistor ladder circuit. Moreover, it allows a complete high-speed A/D converter to be implemented using the standard CMOS logic technology, making the featured A/D converter ideal

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for SOC implementation.

The design and simulation results of a 6-bit flash A/D converter with TIQ technique are presented in this paper. Section 2 describes in detail the proposed A/D converter architecture and TIQ comparators. Section 3 describes the layout method for optimal speed and for overcoming the process variation. Finally, Section 4 describes the simulation results obtained.

2. A/D Converter Design

Figure 1 shows the block diagram of the proposed TIQ based 6-bit flash A/D converter with 63 comparators, 63 gain boosters, and an encoder. The voltage comparators compare the input voltage with internal reference voltage. The gain boosters make sharper thresholding of comparator output and provide full digital output voltage swing. The encoder converts the thermometer code to the binary code in two steps.

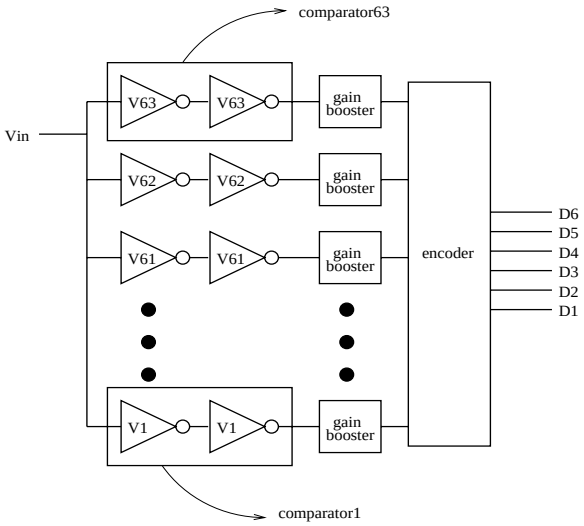
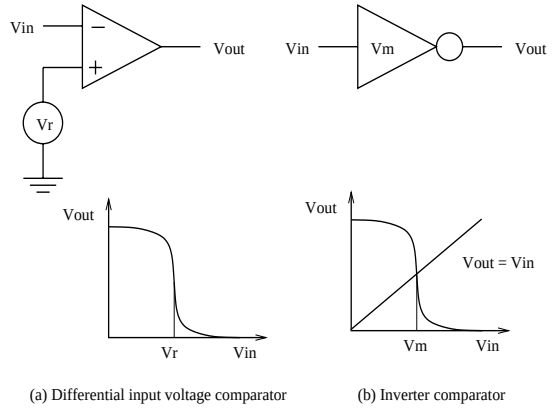


Figure 1. Block diagram of the proposed TIQ based 6-bit flash A/D converter

2.1. Voltage Comparator

Figure 2 shows the similarity and difference between a differential input voltage comparator and an inverter. The inverter circuit is inherently simpler and faster than the differential input voltage comparator circuit. In a conventional flash A/D converter, the differential input voltage comparators are used and the reference voltage V_r is generated by the resistor ladder circuit.

On the other hand, the TIQ technique uses a digital inverter circuit as a voltage comparator. With the inverter



(a) Differential input voltage comparator (b) Inverter comparator

Figure 2. The similarity and difference between a differential input voltage comparator and an inverter

comparator, the inverter switching threshold voltage V_m is internal to the inverter, fixed by the transistor sizes. The inverter switching threshold voltage V_m is defined at $V_{in} = V_{out}$ point on the voltage transfer characteristic curve of an inverter. The authors obtained the equally spaced inverter switching threshold voltages between maximum V_m (comparator 63 in Figure 1) and minimum V_m (comparator 1 in Figure 1) by systematically changing the transistor sizes.

In a conventional flash A/D converter, the 2^n voltage comparators are identical, using the resistor ladder circuit to generate 2^n reference voltages to compare. In the TIQ based flash A/D converter, the 2^n voltage comparators are different and the 2^n reference voltages are built-in to the comparators. Designing the 2^n different voltage comparators can be a difficult task; however, the authors were able to design and redesign many times without difficulty using the modern VLSI CAD tools.

The TIQ technique has many advantages:

- Simpler voltage comparator circuit
- Faster voltage comparison speed
- Elimination of resistor ladder circuit
- Does not require switches, clock signal, or coupling capacitors for the voltage comparison.
- Suitable for the standard CMOS technology, ideal for the SOC implementation.
- Highly adaptable to future CMOS technology development, going to smaller feature size and lower supply voltage.

The following two criteria must be carefully considered to obtain a successful TIQ based A/D converter implementation:

(1) ADC input range varies due to process parameter changes from one fabrication to another.

(2) An inverter input is single ended, not differential, causing the ADC to become more susceptible to noise.

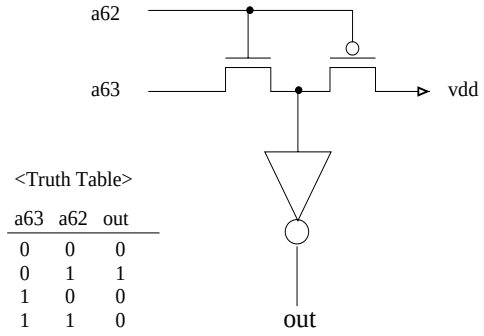
As a working solution for criterion (1), one may add a programmable pre-amplifier to the signal input of the TIQ based ADC to adjust signal offset and amplitude. To correct (2), one may implement the inverters in highly isolated substrate from the digital circuits. The combination of a well-designed layout strategy, a deep trench isolation method, and a separate analog power supply may significantly minimize the effects of noise.

2.2. Gain Booster

Each gain booster consists of two cascading inverters with the same circuit as the comparator, except that the transistor sizes of each gain booster are smaller and identical to each other. The gain boosters make sharper thresholding of comparator output and provide full digital output voltage swing.

2.3. Encoder

The encoder converts the thermometer code to the binary code in two steps. The thermometer code is converted to the 1-out-of-n code, using the '01' generators. This code is then converted to binary code. Figure 3 shows a single cell optimized '01' generator circuit using only four transistors, providing full swing output in a small layout area. For the 6-bit A/D converter, 63 '01' generator cells are used in parallel to generate 1-out-of-63 code.



<Truth Table>

a63	a62	out
0	0	0
0	1	1
1	0	0
1	1	0

Figure 3. The optimized '01' generator circuit

To convert the 1-out-of-63 code to the binary code, a ROM is used. An optimized NOR ROM circuit was developed by the authors to achieve high speed conversion. For the proposed TIQ based A/D converter, the ROM speed is the predominant factor in overall A/D conversion speed. In future, the TIQ based A/D converter can be improved by alternate faster non-ROM based encoder design such as [3].

3. Layout

Careful layout design is important for speed increase and area reduction. Also, a good layout strategy can significantly minimize the effects of noise and process variation. Figure 4 shows the optimized layout of the 6-bit TIQ based flash A/D converter with 0.25 μm standard CMOS design rule. The left half of the layout is the 63 TIQ comparators, and right half is the 63 gain boosters, plus the encoder circuit.

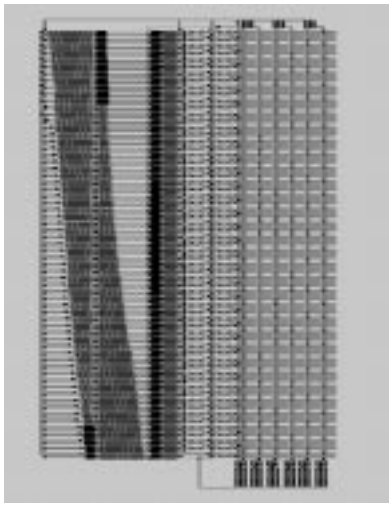


Figure 4. Layout of the 6-bit A/D converter

4. Simulation Results

Simulation was performed using 0.25 μm standard CMOS technology parameters. The DC analysis of the 63 TIQ comparator outputs is shown in Figure 5. One may notice the uniformity of 63 equally spaced inverter voltage transfer curves.

To see the process variation effects on the 6-bit TIQ based A/D converter, Figure 6 shows the transient analysis results of six different process parameters. One can see the input voltage graph on the first row at each process in Figure 6. At least 65 input steps were applied to the 6-bit TIQ based A/D converter input for transient analysis. The A/D converter operates at the speed of 1 Gigasamples per second (GSPS) shown in Figure 6 (a). The input interval including sampling time and holding time is 1 ns for 65 input voltages, leading to 65 ns for operation without any missing code. The simulation result and other features are summarized in Table 1.

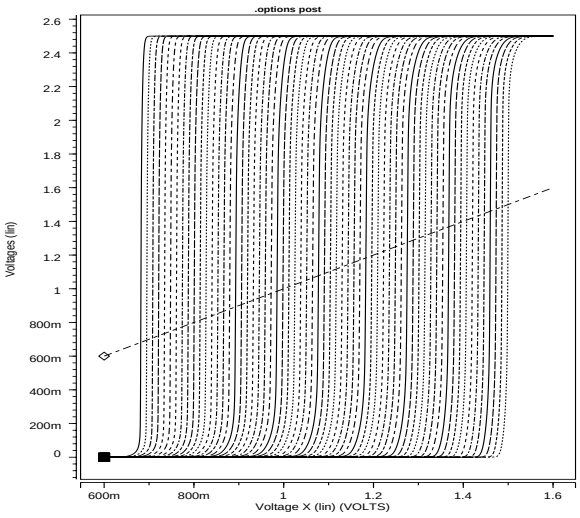


Figure 5. DC analysis of the 63 TIQ comparator outputs

Table 1. Simulation results for the 6-bit A/D converter

CMOS technology	0.25 μm
Power supply	2.5 V
Speed	1 GSPS
Area	0.013 mm^2
Avg. power consumption	44.34 mW
Max. power consumption	66.87 mW
V_m range	0.6815 V - 1.4999 V
V_m distance	0.0132 V

The rest of the Figure 6 show the effects of the process parameter variation. The results of five different process parameters are similar to that of the first one (n94s). As one can see in Figure 6, all results show correct operation without any missing codes, but the authors found shifting and expanding (or contracting) in the A/D converter operation voltage ranges, shown in Table 2. To tolerate the process parameter variation, one may add a programmable preamplifier to the signal input of the TIQ based A/D converter, thereby adjusting signal offset and amplitude.

Table 3 shows the comparison of the proposed 6-bit TIQ based CMOS A/D converter with other A/D converters. Clearly the proposed TIQ based CMOS A/D converter has the potential for ultrafast speed, all-CMOS, and low-power features that are suitable for SOC applications.

5. Conclusion

A simple and fast A/D converter architecture that uses inverter comparator for flash A/D conversion, named TIQ technique, has been proposed. The 6-bit TIQ based flash A/D converter designed for the standard digital CMOS technology has ultrafast sampling rate of 1 GSPS.

The simulation results show that the process parameter variation does not cause missing code or significant nonlinearity in conversion range. Nevertheless, the problem of shifting and expanding/contracting of the input voltage range exists, for which there is a practical solution.

The TIQ based A/D converters are preferable for SOC implementation. Also it is highly adaptable to future CMOS technology development, going to smaller feature size and lower power supply voltage.

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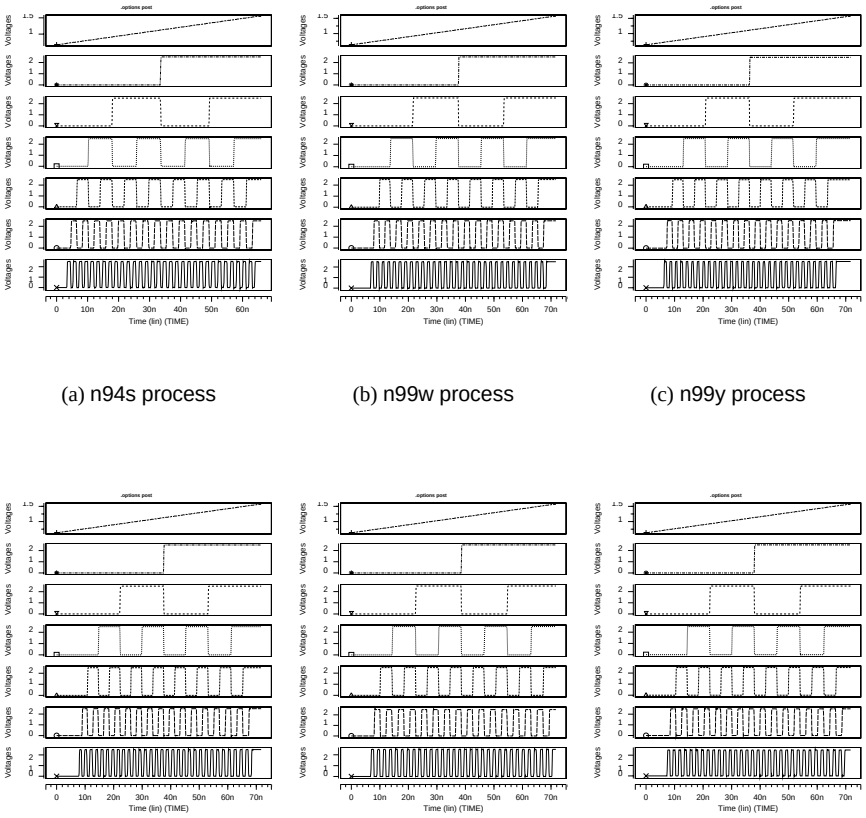

(a) n94s process (b) n99w process (c) n99y process

(d) n9bm process (e) t02b process (f) t02d process

Figure 6. Transient analysis for 6 processes

Table 2. The change of A/D converter operation voltage ranges due to the process variation

Process	Start V_m	End V_m	Range	Avg distance	Max power	Avg power
n94s	0.6815 V	1.4999 V	0.8184 V	0.0132 V	66.87 mW	44.35 mW
n99w	0.6911 V	1.5030 V	0.8119 V	0.0131 V	64.53 mW	40.46 mW
n99y	0.6819 V	1.4808 V	0.7989 V	0.0129 V	65.97 mW	41.57 mW
n9bm	0.6984 V	1.4983 V	0.7999 V	0.0129 V	65.30 mW	41.70 mW
t02b	0.6874 V	1.5288 V	0.8414 V	0.0136 V	72.29 mW	46.51 mW
t02d	0.6955 V	1.5188 V	0.8233 V	0.0133 V	71.48 mW	45.29 mW

Table 3. The comparison of the proposed 6-bit TIQ based CMOS A/D converter with other A/D converters

ADCs	Resolution	Sampling rate	Technology	Gate length	Type	Power
Proposed	6-bit	1 GSPS	CMOS	0.25 μm	Flash	66.87 mW
[1]	6-bit	2 GSPS	GaAs	0.5 μm	Flash	970 mW
[2]	6-bit	0.2 GSPS	CMOS	0.6 μm	Flash	380 mW
[5]	4-bit	1.18 GSPS	GaAs	0.8 μm	Flash	185.6 mW
[6]	6-bit	0.5 GSPS	CMOS	0.4 μm	Flash	400 mW
[9]	8-bit	0.15 GSPS	CMOS	0.6 μm	Pipeline	395 mW
[10]	6-bit	0.5 GSPS	CMOS	0.6 μm	Flash	330 mW