A SINGLE-PIECE CHARGE-BASED MODEL FOR THE OUTPUT CONDUCTANCE OF MOS TRANSISTORS

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Abstract

This paper presents a physically based model of the MOSFET output conductance. The drain current and the output conductance of the MOS transistor are accurately described by single-piece functions of the inversion charge densities at source and drain. Carrier velocity saturation, channel length modulation (CLM) and drain induced barrier lowering (DIBL) are included in a single-piece analytical model. The results herein can be readily applied for first order analog circuit hand calculation.

1. Introduction

Almost all the MOSFET models included in circuit simulators use the regional approach and some non-physical curve interpolation to bridge the linear and saturation regions [1-4]. A good MOSFET model should exhibit continuity not only in the drain current but also in the output conductance. The effects of carrier velocity saturation, CLM, DIBL and substrate current induced body effect (SCBE) must be taken into account to calculate the output conductance of a MOSFET.

In the classical approach to model the saturation region, the output conductance is assumed to be proportional to the (saturation) drain current and inversely proportional to the Early voltage V_A [1], a constant parameter in first order models such as SPICE1. However, it is widely known that a constant Early voltage is inadequate to model the output conductance for the simulation of analog circuits. Other models [2,4,11] use smoothing functions to unify the linear and saturation regions. However, they demand the extraction of parameters which neither have a simple physical interpretation nor are easy to extract. Another drawback of some simulators is that the carrier velocity saturation model is only valid in strong inversion [1, 2 , 5, 6], but not in weak inversion, where the channel is almost equipotential [1]. Consequently, saturation is modeled with a physical background in strong inversion while, on the other hand, it is defined in an empirical manner [5, 8] in weak and moderate inversion.

This paper presents a charge-based physical model of the MOSFET output conductance, valid from weak to strong inversion. Our model includes velocity saturation effects, CLM and DIBL. Impact ionization effects can be easily included in our model by adding a substrate current such as in [2]. A physical definition of the MOSFET output conductance in terms of a saturation charge is proposed. From the basic definition of saturation charge, alternative definitions of saturation in terms of current or voltage can be derived. A simple expression for the output conductance showing its dependence on bias is given.

2. MOSFET charge-based current model

The basic assumption of our model is the linear dependence of the inversion charge density Q'_I on the surface potential ϕ_S [7, 9], for a given gate-to-bulk voltage (V_G):

$$dQ'_I = nC'_{ox}d\phi_S \tag{1}$$

where C'_{ox} is the oxide capacitance per unit area and n is the slope factor, slightly dependent on the gate voltage.

The effect of velocity saturation in our model is based on the expression [7] below:

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$$\mu_S = \frac{\mu}{1 + \frac{\mu}{v_{lim}} \frac{d\phi_S}{dx}} \quad (2)$$

where the mobility μ is a function of the gate -to-bulk potential V_G only and v_{lim} is the saturation velocity.
The substitution of both the approximations (1) and (2) into the differential equation of the drain current leads, after integration along the channel, to [7,8]

$$I_D = \frac{\mu W_{eq}}{C'_{ox} L_{eq}} \frac{1}{1 + \frac{|Q'_{IS} - Q'_{ID}|}{Q'_A}} \frac{\left[Q'^2_{IS} - Q'^2_{ID} - 2nC'_{ox}(Q'_{IS} - Q'_{ID})\right]}{2n} \quad (3)$$

where

$$Q'_A = n.C'_{ox}.L_{eq}.U_{CRIT} \quad \text{and} \quad U_{CRIT} = \frac{v_{lim}}{\mu} \quad (4)$$

ϕ_t is the thermal potential and L_{eq} is the transistor electrical length.
The charge-based expression (3) to calculate the drain current includes the effects of diffusion, drift and carrier velocity saturation. (3) is a general expression that is valid from weak to very strong inversion. The charge in the denominator models velocity saturation; the term $|Q'_{IS} - Q'_{ID}|$ correctly represents the channel potential in strong as well as in weak inversion.

3. Operation in saturation

The maximum current that can flow in the channel occurs when the maximum velocity in the inversion layer reaches the saturation velocity. In this case:

$$I_D = -W v_{lim} Q'_{ID} \quad (5)$$

Equating (3) to (5) allows one to calculate Q'_{IDSAT}, the value of Q'_{ID} which corresponds to the onset of saturation:

$$Q'_{IDSAT} = Q'_{IS} - nC'_{OX}\phi_t - Q'_A\left[1 - \sqrt{1 - \frac{2(Q'_{IS} - nC'_{OX}\phi_t)}{Q'_A} + \frac{(nC'_{OX}\phi_t)^2}{Q'^2_A}}\right] \quad (6)$$

Equation (6) is a general definition, for any inversion level, of the MOSFET inversion charge at the onset of saturation. (6) can be readily interpreted if one assumes $|Q'_{IS}| << Q'_A$. This inequality is valid for all inversion conditions but very strong inversion. In this case, (6) can be approximated by a second order power series:

$$Q'_{IDSAT} = \frac{\phi_t}{U_{CRIT}.L_{eq}}\left(1 - \frac{Q'_{IS}}{2nC'_{ox}\phi_t}\right)Q'_{IS} \quad (7)$$

Eqn.(7) shows that the saturation charge is a very small fraction, equal to $\phi_t/(U_{CRIT}.L_{eq})$, of the inversion charge at source in weak inversion ($|Q'_{IS}| << nC'_{ox}\phi_t$). For moderate and strong inversion, the saturation charge is a larger fraction of Q'_{IS} but is still much smaller than Q'_{IS} as long as $|Q'_{IS}| << Q'_A$.
Expressing the inversion charge density Q'_{IS} at source in terms of the drain current by means of (3) and using the approximation $|Q'_{IS}| << Q'_A$, (7) can be rewritten as

$$\frac{Q'_{IDSAT}}{Q'_{IS}} \cong \frac{\phi_t}{U_{CRIT}.L_{eq}} \frac{\sqrt{1+i_d}+1}{2} \quad (8)$$

where $i_d = I_D/I_S$ is the normalized saturation current and

$$I_S = \mu n C'_{ox} \frac{W}{L}\frac{\phi_t^2}{2} \quad (9)$$

is the normalization current [10].
Recalling the charge-voltage relationship from [4,10]:

$$\frac{V_P - V_{S(D)}}{\phi_t} = \frac{Q'_{IP} - Q'_{IS(D)}}{nC'_{ox}\phi_t} + \ln\left(\frac{Q'_{IS(D)}}{Q'_{IP}}\right) \quad (10)$$

V_{DSSAT}, the drain-to-source voltage for which the maximum velocity of the carriers is equal to the saturation velocity, can be calculated as

$$V_{DSSAT} \cong \phi_t\left[\ln\left(\frac{U_{CRIT}.L_{eq}}{\phi_t}\right) + \sqrt{1+i_d} - 1\right] \quad (11)$$

In (10) V_P and Q'_{IP} are the pinch-off voltage and the inversion charge density at pinch-off [4,10], respectively. To obtain (11) the ln term in (10), which prevails in weak inversion, has been considered constant for any drain current and equal to its value deep in weak inversion.
Eqns.(8) and (11) are alternative descriptions of MOSFET saturation owing to the effect of the carrier velocity saturation. (8) and (11) are valid from weak to strong inversion and clearly show the effect of bias (current level) on the saturation characteristics. The saturation voltage does not depend on the current for low current levels ($i_d <<1$) and is proportional to the square root of the current for high current levels ($i_d>>1$). For very strong inversion (8) and (11) are no longer valid and (6) should be used to calculate the correct saturation charge.

4. MOSFET output conductance in saturation

In analog circuits MOSFETs frequently operate in the saturation region, where the transistor voltage gain can be made large. Explicit expressions of the output conductance in that region are useful for design purposes. We are going to show now how to use the results from the previous section in order to calculate the MOSFET output conductance.
From (5) one can write:

$$g_d = \frac{dI_D}{dV_D} = -Wv_{lim}\frac{dQ'_{IDSAT}}{dV_D} \quad (12)$$

The saturation charge Q'_{IDSAT} depends on the channel length, L_{eq}, and on the inversion charge density at source, Q'_{IS}. At this point we can include both the CLM and DIBL effects to calculate the small-signal output conductance. The channel length is generally written as $L_{eq} = L - \Delta L$, where ΔL is the channel shrinkage. Many models have been tried to describe CLM [11]. Here we model the CLM as in [5]

$$\Delta L = \lambda . L_C \ln\left[1 + \frac{V_{DS} - V_{DSSAT}}{L_C . U_{CRIT}}\right] \quad (13)$$

where λ and L_C can be considered as fitting parameters. The DIBL effect is represented in our model by the DIBL parameter, σ, which models the dependence of the pinch-off voltage, V_P, on both the drain and source voltages according to:

$$V_P(V_G, V_S, V_D) = V_{P0}(V_G) + \frac{\sigma}{n}(V_D + V_S) \quad (14)$$

Now, (12), (13) and (14), together with (7) and (10), can be used to calculate the MOSFET output conductance to current ratio:

$$\frac{g_d}{I_D} = \frac{1}{V_A} = \frac{\lambda}{U_{CRIT} . L_{eq}} . \frac{1}{1 + \frac{V_{DS} - V_{DSSAT}}{L_C . U_{CRIT}}} + \frac{\sigma}{n\phi_t}\frac{2}{\sqrt{1 + i_d} + 1} \quad (15)$$

Eqn.(15) is a generalization, for any bias conditions, of the MOSFET output conductance presented in [6]. One can readily notice that the CLM component of V_A, the Early voltage, depends only on the effective voltage drop across the shrunk part of the channel while the DIBL component depends on the current level i_d. The Early voltage is independent of the current level for weak inversion and increases in moderate inversion. For higher inversion levels the DIBL component of the Early voltage can be neglected compared to the CLM component.

From the above results it becomes clear that the new model (15) of the Early voltage proposed here includes the conventional Early voltage formulation as a limit case. (15) is valid as long as $|Q'_{IS}| << Q'_A$.

5. Results

MOSFETS from a 0.75μm technology with different channel lengths were measured for several bias conditions. Fig.1 displays the output characteristics of two MOSFETS with different channel lengths. The characteristics of the MOSFET with minimum channel length (L=0.75μm) are strongly affected by the DIBL effect in the weak inversion region.

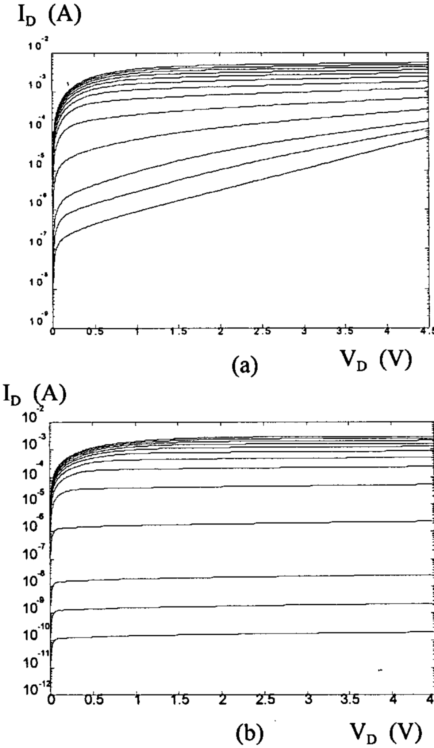

Fig. 1. Output characteristics of NMOS transistor for V_G = 0.5, 0.6, 0.7, 0.9, 1.2, 1.6, 2.0, 2.4, 2.8, 3.2, 3.6, 4.0, 4.4 V a) L = 0.75μm and b) L = 1.25μm

From Fig.2 we can conclude that the Early voltage increases with increasing lengths, is independent of the current level in weak inversion and increases in moderate and strong inversion as predicted by (15).

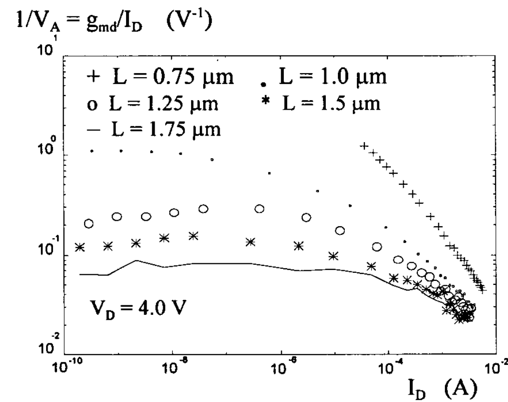

Fig.2. The output conductance to current ratio of NMOS transistors with channel length varying from 0.75μm to 1.25μm

Fig.3 shows that the Early voltage is almost independent of V_D in weak inversion. The comparison of Fig 3 a) and 3 b) shows that for the transistor with L=0.75µm the DIBL component of V_A is dominant and the CLM component becomes important as the channel length increases.

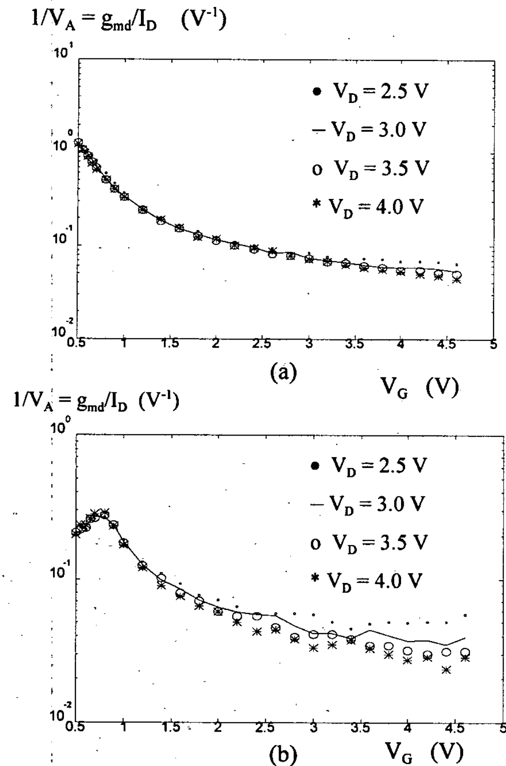

Fig.3. The output conductance to current ratio versus gate voltage with V_D varying from 2.5V to 4.0V of NMOS transistors with a) L=0.75µm and b) 1.25µm

6. Conclusions

A compact charge-based model for the output conductance of the MOSFET has been presented. Some advantages of our model over BSIM3v3 are the use of simple expressions to describe all regions of operation as well as a smaller number of device parameters. The present model includes the conventional Early voltage formulation as a limit case and allows the calculation of the Early voltage in terms of physical parameters as well as bias conditions.

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